REMARKS

Claims 1, 3, 5-9, 13-15 and 21-31 are pending in this application. By this Amendment, claim 28 is canceled.

Counsel thanks the Examiner for his courtesies extended during the telephone discussions had before issuance of the outstanding action. Subsequent to those discussion, the undersigned contacted one of the inventors of the present application to discuss the issues raised by the Examiner. Unfortunately, the undersigned and the Examiner were not able to connect prior to issuance of the Office Action.

The withdrawal of the rejection of original claims 2, 3, 6, 7, 16 and 18 under 35 U.S.C. 112, first paragraph, and the rejection of claims 1-20 under 35 U.S.C. 112, second paragraph, is greatly appreciated.

The outstanding Office Action repeats the rejection of claims 13, 14, 21 and 28 under 35 U.S.C. 112, first paragraph, as allegedly being not enabled by the disclosure.

In reply, the following comments are submitted. The Office Action indicates that the specification suggests that the different memory arrays "somehow simultaneously drive data onto a common signal line such that the two memory responses may be distinctly resolved." However, in order to practice the invention as described in these claims it is not necessary that the data from two or more memory arrays be driven onto a common signal line at the same time. For example, as described on page 2 of the specification, lines 3-15, with respect to the prior art depicted in Figures 1(a) and 1(b), when a data byte 22 is read out, a plurality of bits 20 are retrieved, one bit from each of the eight arrays, such that each bit is routed on data bus 8 making up byte 22. The data bus 8 is eight bits wide as described in the specification at line 8 of page 2. The eight instances of memory arrays 4 shown in Figures 1(a) and 1(b), as described in the example in the specification, output one bit in response to a memory access command. It is well known in the art in a configuration such as that shown in Figures 1(a) and 1(b), that the data bus will have a plurality of separate (e.g., eight) data lines, each data line connected to a different one of the memories.

In the context of the various embodiments of the present invention described in connection with the latter figures in the present application, similar well known signal routing techniques would be applied between the two or more dissimilar memory arrays and the memory

controller. One with ordinary skill in the art would understand that the data bus would have a plurality of signal lines, where separate signals lines would be dedicated to carrying data from the respective memories. Using these techniques, it is therefore possible to route signals from the two or more memory arrays simultaneously on different lines of a common data bus. Thus, a portion of a data byte can arrive at the memory controller at substantially the same time along the common data bus, but of course, on different signal lines of the data bus. Thus, using this signal routing technique, the data bits from the different memory arrays would not be simultaneously driven on the same signal line.

The foregoing is only one technique that may be used to practice the present invention. Other techniques are known in the art, though for purposes of the understanding the basic principles of the invention, it is respectfully submitted that it is not necessary that they be explained in such detail in the specification for the present application.

For these reasons, it is respectfully submitted that claims 13, 14, 21 and 28 are enabled under 35 U.S.C. 112, first paragraph, and that the rejection on these grounds be withdrawn.

The Office Action rejects claim 28 under 35 U.S.C. 112, second paragraph, as being allegedly indefinite. Claim 28 has been canceled without prejudice or disclaimer. Therefore, this rejection is now moot.

The Office Action rejects claims 1, 3, 5-9, 13-15 and 21-31 under 35 U.S.C. 102(b) as allegedly being anticipated, or in the alternative, under 35 U.S.C. 103(a) as being allegedly obvious, over Benini et al. (hereinafter "Benini").

Independent claims 1, 18 and 15 have been amended to clarify that the two or more memory arrays are implemented in the same integrated circuit chip.

Benini relates to automatic generation of a multi-bank memory architecture for embedded systems, and particularly to synthesizing a multi-bank memory architecture optimally fitted to an execution profile of an embedded application that runs on a given processor core. Benini further describes in his section 3.2 a partitioning tool that can, for a given number of words, produce different memory configurations using memories of different features in terms of "shapes of the memory (different aspect ratios), delays and power dissipation."

However, as recited in independent claims 1, 8 and 15, Benini does not teach or suggest the concept of providing at least first and second memory arrays on the same integrated circuit

chip, where the first and second memory arrays have dissimilar operating characteristics (but are addressed using a common addressing scheme) such that one of the arrays operates faster than the other of the arrays during a read or write operation, and such that the memory arrays are operated in conjunction with one another when reading data from them or writing data to them. Benini does not teach or suggest that the memory arrays are addressed using a common addressing scheme. This aspect, which appears in all of the independent claims, is completely ignored in the Office Action.

As recited in claims 3 and 25, Benini does not teach or suggest at least two memory arrays that operate at different operating or supply voltages such that one of the arrays operates faster than the other, where the faster array is connected to a memory controller with a longer signal path than the signal path that connects the slower array to the memory controller.

As recited in claims 5 and 26, Benini does not teach or suggest at least two memory arrays, specifically that one has a shorter wordline length than the other, and specifically that the memory array having the shorter wordline length is connected to a memory controller by a signal path that is shorter than the length of the signal path that connects the memory array with the longer wordline length.

As recited in claims 7, and 27, Benini does not teach or suggest at least two memory arrays, and specifically that one has sensing circuitry driven by a system supply voltage and the other of which has sensing circuitry driven by a ground potential such that one of the arrays has a faster cycle time than the other, but has a longer latency interval than the other. Further, as recited in claim 21, Benini does not teach or suggest specifically that multi-byte information is read out from the arrays by reading a first byte from one array, followed by a second byte from the other array and followed by a third byte from the other array.

Benini does not teach or suggest at least two memory arrays: specifically that one of which has a refresh rate and refresh current that is greater than a refresh rate and refresh current of the other array (claims 22 and 29); specifically that one of which has more cells per bitline than the other array (claims 23 and 30) and one of which has at least two sub-arrays, each having the same number of cells per bitline (claims 24 and 31).

In sum, Benini fails to anticipate or render obvious the concepts described in the independent as well as the dependent claims. While the Office Action draws from general

excerpts taken from Benini, it is respectfully submitted that Benini does not anticipate nor render obvious the subject matter of the claims. It is respectfully submitted that the anticipation and apparent obviousness analyses in the Office Action based on Benini improperly use hindsight; the subject matter of the present application (as claimed and described) should not be read into the prior art.

Based upon the foregoing, it is respectfully submitted that the present application is condition for allowance. Should the Examiner have any questions or comments, he is cordially invited to telephone the undersigned so that the present application may receive a prompt Notice of Allowance.

No extension of time or other fees are believed to be due. However, Applicants hereby petition for any extension of time that may be necessary to maintain the pendency of this application. The Commissioner is hereby authorized to charge payment of any additional fees required for the above-identified application or credit any overpayment to Deposit Account No. 05-0460.

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